DATA SHEET

TDA8707
Triple RGB 6-bit video analog-to-digital interface

Product specification
Supersedes dat of March 1995
File under Integrated Circuits, IC02

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Philips
Semiconductors

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Triple RGB 6-bit video analog-to-digital interface

TDA8707

FEATURES

- Triple analog-to-digital converter (ADC)
- 6-bit resolution
- Sampling rate up to 35 MHz
- Power dissipation of 335 mW (typical)
- Internal clamping function
- TTL compatible digital inputs
- –40 to +85 °C operating temperature
- CMOS digital outputs.

APPLICATIONS

- High-speed analog-to-digital conversion for video signals
- VGA signal treatment.

DESCRIPTION

The TDA8707 is a CMOS triple 6-bit video low-power analog-to-digital converter (ADC) for RGB signals. It converts the analog inputs into 6-bit binary coded digital words at a sampling rate of 35 MHz. All analog signal inputs are clamped.

Analog-to-digital converter

The TDA8707 implements 3 independent 6-bit analog-to-digital converters in CMOS process. These converters use a full-flash approach.

Clamping feature

An internal clamping circuit is provided in each of the 3 analog channels. The analog pins INR, ING and INB are switched, through series capacitors, to on-chip clamping levels during an active pulse on the clamp input CLP. Clamping level in the R, G and B channels is Code 0.

Input buffers

Internal buffers are provided to drive the analog-to-digital converter inputs. Their ratio can be adjusted externally at 1.5 or 2.0 with select input SLT.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current		–	60	80	mA
I_{DDD}	digital supply current	f_{clk} = 35 MHz	–	5	8	mA
INL	integral non-linearity	f_{clk} = 35 MHz; ramp input; T_{amb} = 25 °C	–	±0.35	±0.6	LSB
DNL	differential non-linearity	f_{clk} = 35 MHz; ramp input; T_{amb} = 25 °C	–	±0.35	±0.6	LSB
EB	effective bits	note 1	–	5.3	–	bits
f_{clk}	maximum clock conversion rate		35	–	–	MHz
P_{tot}	total power dissipation	f_{clk} = 35 MHz; note 2	–	335	485	mW

Notes

1. The number of effective bits is measured with a clock frequency of 35 MHz. This value is given for a 4.43 MHz frequency on the R, G and B channels.
2. The external resistor (value 15 kΩ) between V_{DDA} and CLREF, fixing internal static currents, influences P_{tot}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8707H	QFP44	plastic quad flat package; 44 leads; lead length 1.3 mm; body 10 × 10 × 1.75 mm	SOT307-2

BLOCK DIAGRAM

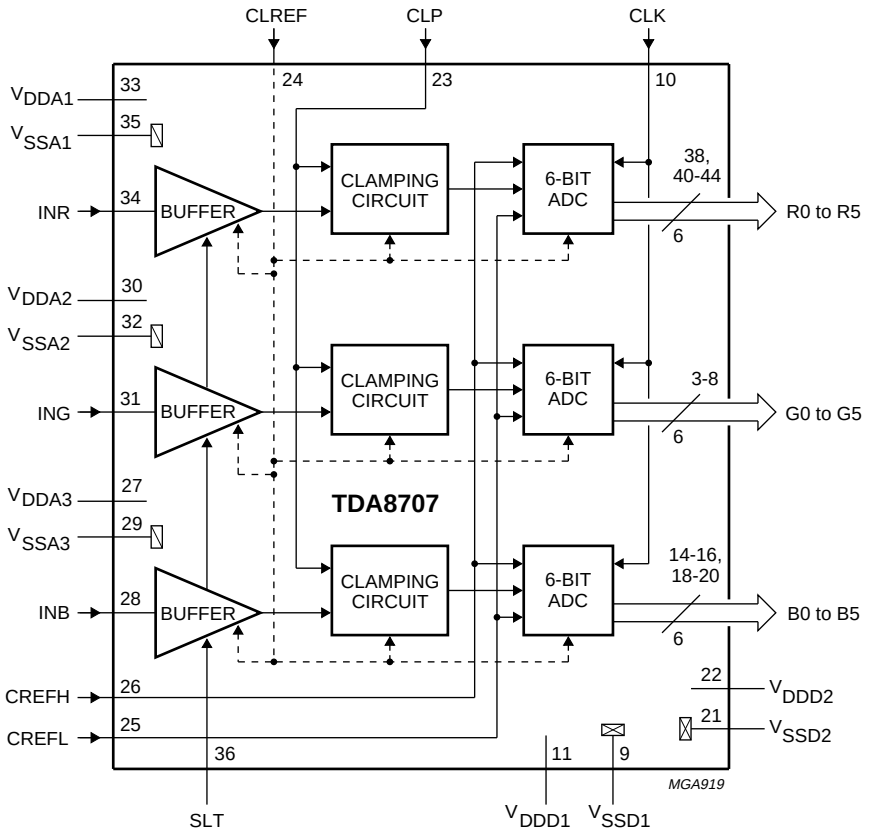


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
G0	3	GREEN data output; bit 0 (LSB)
G1	4	GREEN data output; bit 1
G2	5	GREEN data output; bit 2
G3	6	GREEN data output; bit 3
G4	7	GREEN data output; bit 4
G5	8	GREEN data output; bit 5 (MSB)
V_{SSD1}	9	digital supply ground 1
CLK	10	clock input
V_{DDD1}	11	digital supply voltage 1
n.c.	12	not connected
n.c.	13	not connected
B0	14	BLUE data output; bit 0 (LSB)
B1	15	BLUE data output; bit 1
B2	16	BLUE data output; bit 2
n.c.	17	not connected
B3	18	BLUE data output; bit 3
B4	19	BLUE data output; bit 4
B5	20	BLUE data output; bit 5 (MSB)
V_{SSD2}	21	digital supply ground 2
V_{DDD2}	22	digital supply voltage 2

SYMBOL	PIN	DESCRIPTION
CLP	23	clamping input
CLREF	24	ADCs current reference level input
CREFL	25	converter reference LOW level input
CREFH	26	converter reference HIGH level input
V_{DDA3}	27	analog supply voltage 3
INB	28	BLUE analog input
V_{SSA3}	29	analog supply ground 3
V_{DDA2}	30	analog supply voltage 2
ING	31	GREEN analog input
V_{SSA2}	32	analog supply ground 2
V_{DDA1}	33	analog supply voltage 1
INR	34	RED analog input
V_{SSA1}	35	analog supply ground 1
SLT	36	select input buffer ratio
n.c.	37	not connected
R0	38	RED data output; bit 0 (LSB)
n.c.	39	not connected
R1	40	RED data output; bit 1
R2	41	RED data output; bit 2
R3	42	RED data output; bit 3
R4	43	RED data output; bit 4
R5	44	RED data output; bit 5 (MSB)

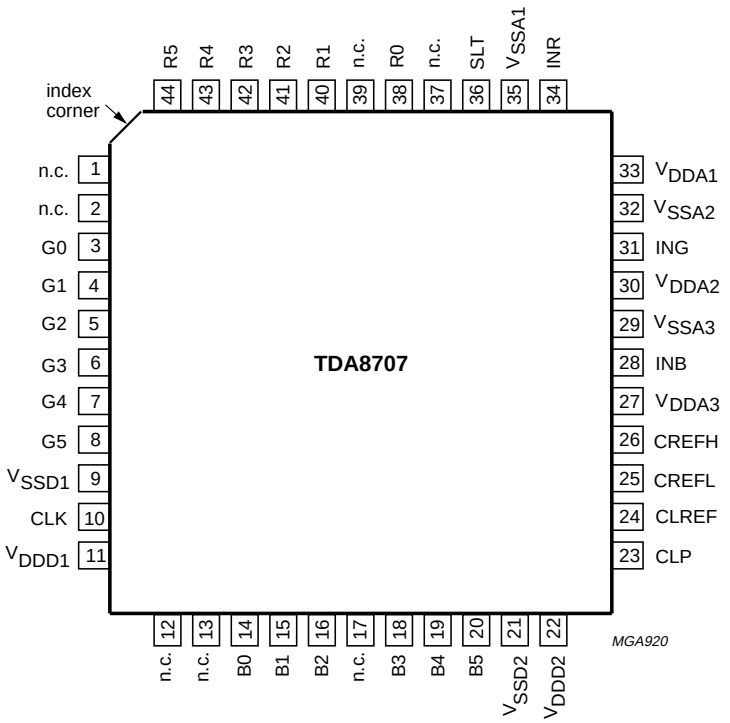


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage (pins 27, 30 and 33)		–0.3	+6.5	V
V_{DDD}	digital supply voltage (pins 11 and 22)		–0.3	+6.5	V
ΔV_{DD}	supply voltage difference between V_{DDA} and V_{DDD}		–0.5	+0.5	V
V_I	input voltage (pins 28, 31 and 34)	referenced to V_{SSA}	–	V_{DDA}	V
$V_{i(p-p)}$	AC input voltage for switching (pins 10 and 23; peak-to-peak value)	referenced to V_{SSD}	–	V_{DDD}	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
T_j	junction temperature		–	+125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	75	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS (see Tables 1 and 2)

$V_{DDA} = V_{DDD} = 4.5$ to 5.5 V; V_{SSA} and V_{SSD} short-circuited together; $V_{DDA} - V_{DDD} = -0.5$ to +0.5 V; $T_{amb} = -40$ to +85 °C; SLT = 0 V; CREFH = 2 V, CREFL = 0.5 V, C_L = 15 pF; typical values measured at $V_{DDA} = V_{DDD} = 5$ V; $V_{SSA} = V_{SSD} = 0$ V and $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage	note 1	4.5	5.0	5.5	V
V_{DDD}	digital supply voltage	note 1	4.5	5.0	5.5	V
I_{DDA}	analog supply current	note 1	–	60	80	mA
I_{DDD}	digital supply current	f_{clk} = 35 MHz	–	5	8	mA
Inputs						
DIGITAL INPUTS (CLK: PIN 10 AND CLP: PIN 23)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DDD}	V
I_{LI}	input leakage current		–10	–	+10	μA
C_I	input capacitance		–	7	–	pF
CLAMP AND REFERENCES (CLREF: PIN 24, CREFL: PIN 25 AND CREFH: PIN 26)						
A_{CL}	clamping accuracy		–	±0.5	–	LSB
I_{CL}	input clamping current		–200	–	+400	μA
C_{CL}	external series clamping capacitor		10	22	–	nF
R_{CLREF}	external resistor on CLREF pin for current reference of converter	note 2	12	15	–	kΩ
V_{REFH}	converter reference voltage HIGH level applied to CREFH pin	referenced to V_{SSA}	1.5	2.0	2.5	V
V_{REFL}	converter reference voltage LOW level applied to CREFL pin	referenced to V_{SSA}	0.25	0.5	0.75	V
ΔREF	reference voltage difference between V_{REFH} and V_{REFL}	note 3	–	1.5	–	V
Z_{CREF}	internal ladder impedance between pins CREFH and CREFL		–	300	–	Ω
ANALOG INPUTS (INR: PIN 34, ING: PIN 31 AND INB: PIN 28)						
$V_{I(p-p)}$	full-range input voltage (peak-to-peak value)	SLT = logic 0; gain = 1.5; note 4	–	1.0	–	V
		SLT = logic 1; gain = 2.0; note 4	–	0.75	–	V
I_I	input current	clamp off	–	5	100	nA
C_I	input capacitance		–	7	15	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
INPUT ISOLATION						
α_{ct}	crosstalk between INR, ING and INB		–	–	–40	dB
Outputs (R0 to R5: pins 38 and 40 to 44; G0 to G5: pins 3 to 8; B0 to B5: pins 14 to 16 and 18 to 20)						
V_{OL}	LOW level output voltage		0	–	0.5	V
V_{OH}	HIGH level output voltage		4.0	–	V_{DDD}	V
Switching characteristics						
CLOCK INPUT CLK (see Fig.3)						
$f_{clk(max)}$	maximum clock frequency		35	–	–	MHz
t_{CPH}	clock pulse width HIGH		10	–	–	ns
t_{CPL}	clock pulse width LOW		12	–	–	ns
Analog signal processing (50% clock duty cycle) f_{clk} = 35 MHz						
LINEARITY						
INL	integral non-linearity	ramp input; T_{amb} = 25 °C	–	±0.35	±0.6	LSB
DNL	differential non-linearity	ramp input; T_{amb} = 25 °C	–	±0.35	±0.6	LSB
BANDWIDTH (see Fig.5 and note 7)						
B	–3 dB analog bandwidth		–	9	–	MHz
t_{STLH}	analog input settling time LOW-to-HIGH	full scale square wave	–	13	16	ns
t_{STHL}	analog input settling time HIGH-to-LOW	full scale square wave	–	11	14	ns
HARMONICS; note 6						
f_1	fundamental harmonic		–	–	0	dB
f_{all}	harmonics, all components		–	–37	–	dB
EFFECTIVE BITS						
EB	effective bits	f_i = 4.43 MHz	–	5.3	–	bits
DIFFERENTIAL GAIN; note 5						
G_{diff}	differential gain	PAL modulated ramp	–	3	–	%
DIFFERENTIAL PHASE; note 5						
φ_{diff}	differential phase	PAL modulated ramp	–	2	–	deg
Timing (see Figs 3 and 4)						
t_{dS}	sampling delay time		–	3	–	ns
t_h	output hold time		6	–	–	ns
t_d	output delay time	note 8	–	–	16	ns
t_r	clock rise time		3	5	–	ns
t_f	clock fall time		3	5	–	ns
t_{CLP}	active clamping duration		3	4	–	µs

Notes to the characteristics

1. V_{DDA} and V_{DDD} should be supplied from the same power supply and decoupled separately.
2. The analog supply current is directly proportional to the series resistance between V_{DDA} and CLREF.
3. CREFH and CREFL are connected respectively to the top and bottom reference ladders of the 3 analog-to-digital converters.
4. $V_{I(p-p)} = (V_{REFL} - V_{REFH})$/buffer gain factor. See Table for gain factor selection. When clamping at code 0 is used, active video signal amplitude V_{ACT} should be: $V_{ACT} = \frac{(V_{REFH} - V_{REFL})}{\text{buffer gain factor}}$
5. Measurement carried out using video analyser VM700A, where the video analog signal is reconstructed through a digital-to-analog converter.
6. $V_{I(p-p)} = \Delta$REF with f_i = 4.43 MHz.
7. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square-wave signal) in order to sample the signal and obtain correct output data.
8. Output data acquisition: output data is available after the maximum delay time of t_d.

Table 1 Typical output coding (V_{REFH} = 2 V; V_{REFL} = 0.5 V referenced to V_{SSA}, SLT = logic 0; buffer ratio = 1.5; T_{amb} = 25°C)

STEP	$V_{I(p-p)}$	BINARY OUTPUT BITS					
		D5	D4	D3	D2	D1	D0
–	$<0.333 = \frac{V_{REFL}}{1.5}$	0	0	0	0	0	0
0	0.349	0	0	0	0	0	0
1	0.364	0	0	0	0	0	1
.	.	.		.	.	.	.
62	1.317	1	1	1	1	1	0
63	1.333	1	1	1	1	1	1
–	$>1.333 = \frac{V_{REFH}}{1.5}$	1	1	1	1	1	1

Table 2 Mode selection

SLT	BUFFER RATIO	TYPICAL $V_{I(p-p)}$ FULL SCALE
0	1.5	$\frac{V_{REFH} - V_{REFL}}{1.5}$
1	2.0	$\frac{V_{REFH} - V_{REFL}}{2.0}$

TIMING DIAGRAMS

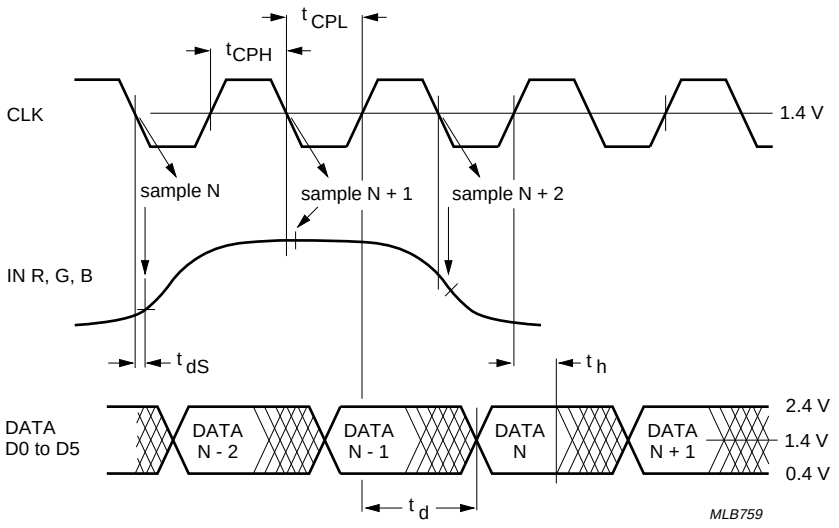


Fig.3 Input timing.

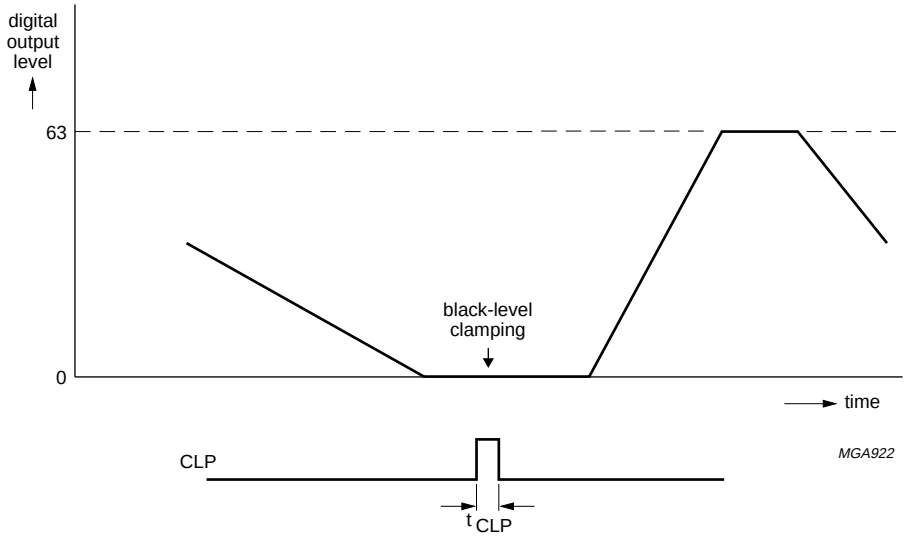


Fig.4 Clamp timing.

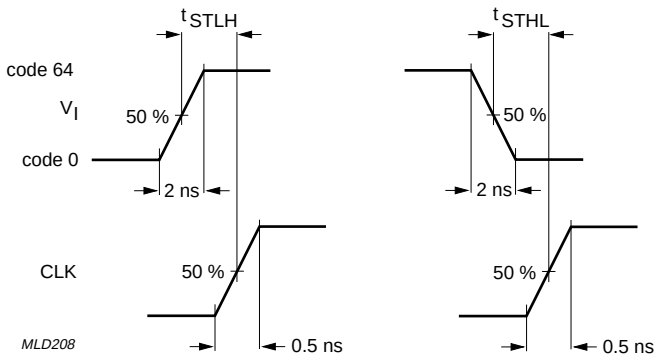
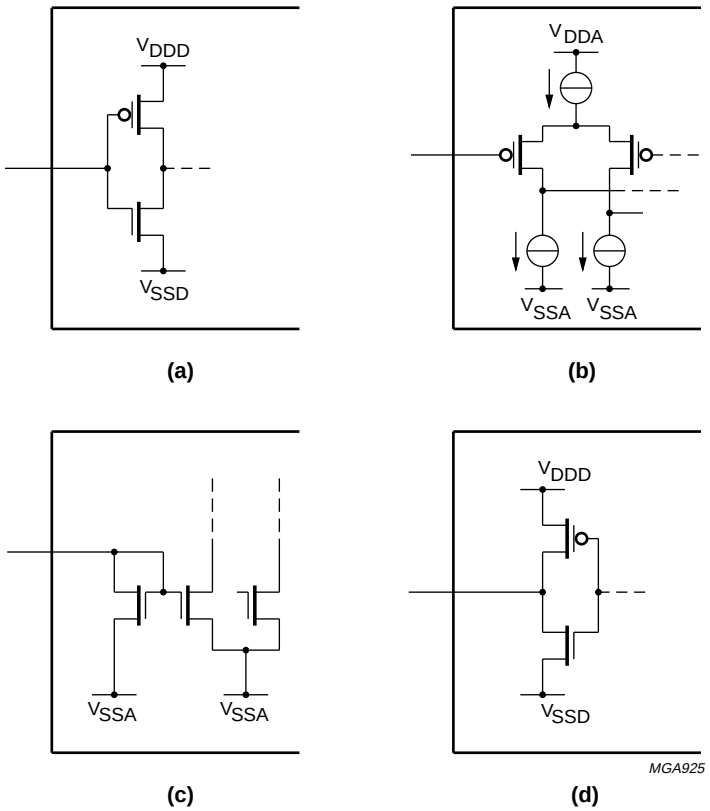


Fig.5 Analog input settling-time diagram.

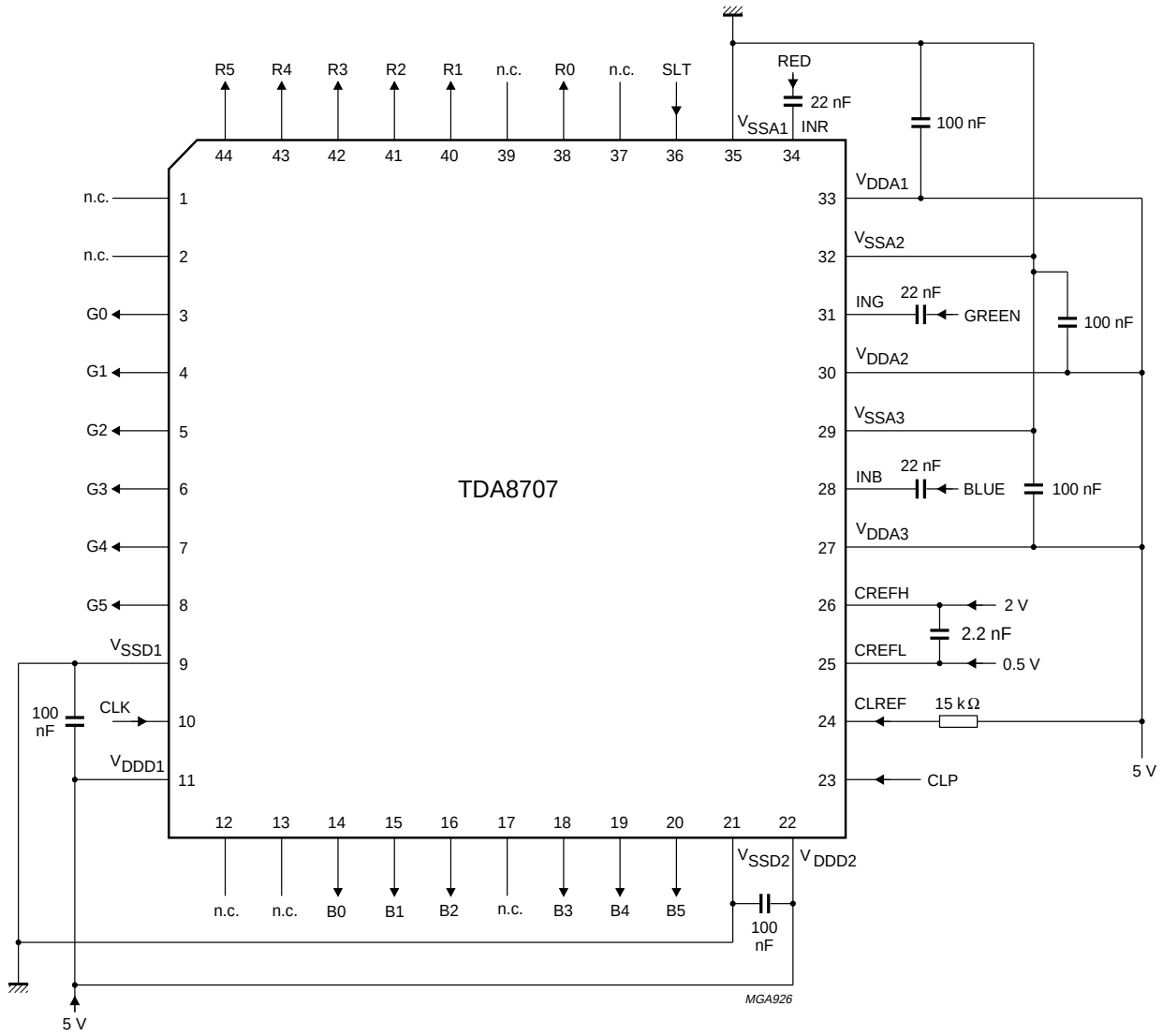
INTERNAL CIRCUITRY



(a) Digital inputs; pins 10, 23 and 36.
(b) Analog inputs; pins 28, 31 and 34.
(c) Current reference; pin 24.
(d) Digital outputs; pins 3 to 8, 14 to 16, 18 to 20 and 40 to 44.

Fig.6 Internal circuitry.

APPLICATION INFORMATION



Analog and digital supplies should be separated and decoupled.

Supplies are not connected internally; also applicable to grounds.

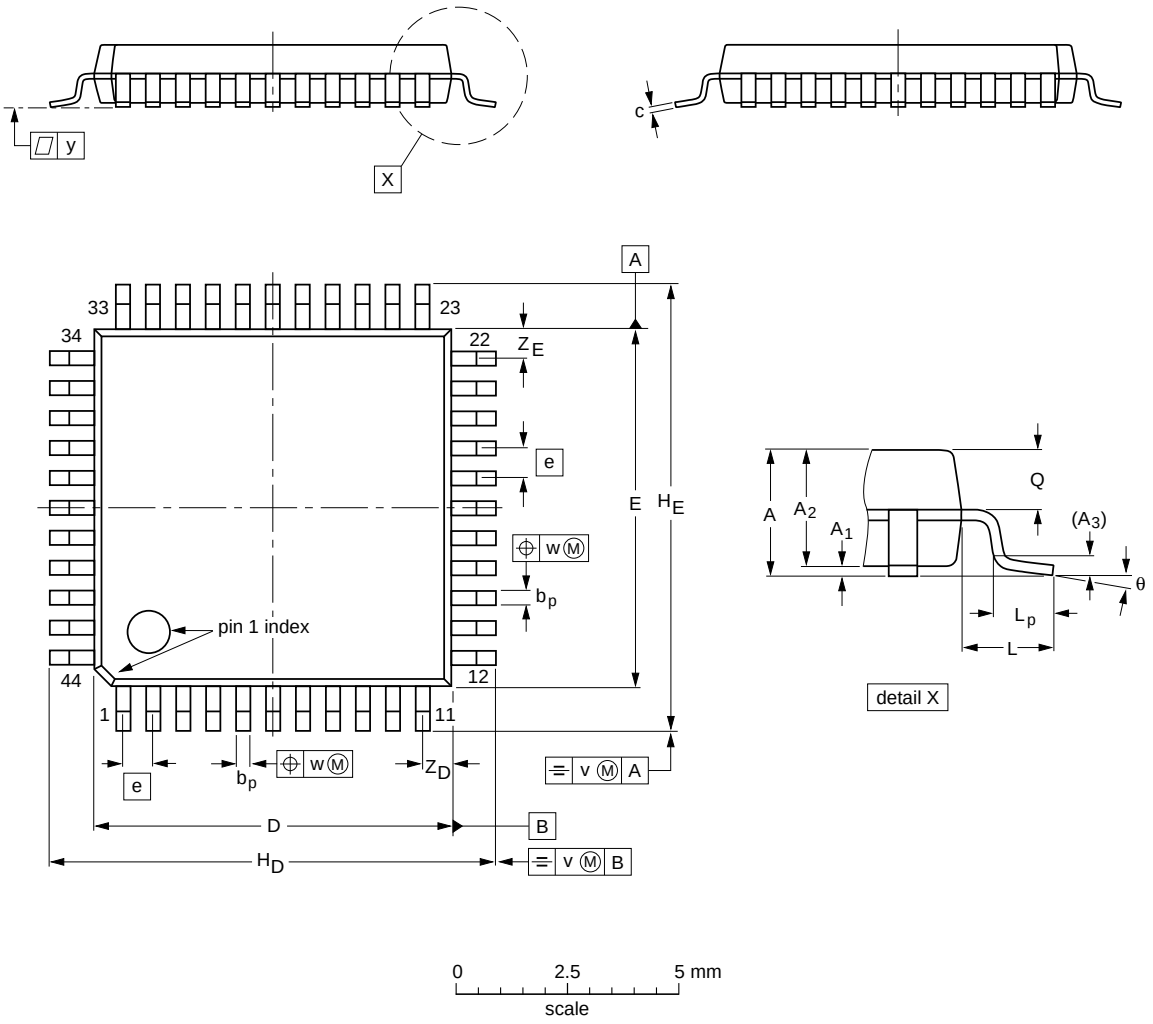
The internal reference currents are set by the series resistor between pin V_{DDA} and CLREF. The resistor value should be in the range of 12 kΩ and 15 kΩ.

It is recommended, if possible, to connect pins 1, 2, 12, 13, 17, 37 and 39 to V_{SSD}.

Fig.7 Application diagram.

PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.85 0.75	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~92-11-17~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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